

**UNITED STATES DEPARTMENT OF COMMERCE****United States Patent and Trademark Office**

Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231

**MF****JS**

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
-----------------	-------------	----------------------	---------------------

09/247,549 02/10/99 KAWAMURA

Y P3213-9008

EXAMINER
----------

WM01/0508

NIKAIDO MARMELESTEIN MURRAY & GRAM  
METROPOLITAN SQUARE  
655 FIFTEENTH STREET N W  
SUITE 330 - G STREET LOBBY  
WASHINGTON DC 20005-5701

YENKE, B	
ART UNIT	PAPER NUMBER

2614

**3**

DATE MAILED:

05/08/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

**on**

# Office Action Summary

Application No.

09/247,549

Applicant(s)

KAWAMURA, YASUNORI

Examiner

BRIAN P. YENKE

Art Unit

2614

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4, 7-9 and 10-12 is/are rejected.
- 7) ☒ Claim(s) 3 and 5-6 is/are objected to.
- 8) ☐ Claims \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 February 1998 is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

- 15) ☒ Notice of References Cited (PTO-892)
- 16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_.
- 18) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_.
- 19) ☐ Notice of Informal Patent Application (PTO-152)
- 20) ☐ Other: \_\_\_\_\_.

Art Unit: 2614

## DETAILED ACTION

### *Specification*

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Drawings*

2. The drawings are objected to because **Fig 4 should have a box around the elements and labeled 6, since it is a detailed figure of calculation circuit 6.**

Correction is required.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 10 recites the limitation "the shift circuit" in line 5. There is insufficient antecedent basis for this limitation in the claim.

### *Claim Rejections - 35 USC § 102*

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2, 8 and 11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by **Ogawa et al., US 4,982,179.**

In considering claims 1-2 and 11-12, Ogawa discloses all the claimed subject matter,

- 1) the claimed a color-difference signal generating circuit for generating a color-difference signal from the RGB signals **is met by matrix 10 (Fig 2; col 3, line 60-65)**
- 2) the claimed a memory for storing values of trigonometric functions covering a predetermined number of cycles at addresses corresponding to evenly spaced phases **is met by cosine and sine function generator 18 and 19 (respectively) of subcarrier generator 15 (Fig 2; col 4, line 53-63) which store sine and cosine function values in accordance with the phase information value  $\theta$  (col 5, line 27-44) where the phase information values can be varied.**
- 3) the claimed an address calculating circuit for calculating addresses at which to access the memory in accordance with the video format actually used **is met by register 17 (Fig 2) of subcarrier generator 15, which receives via adder 16 and VAL 30 the period of the of the subcarrier and the sampling period of the RGB signals (col 4, line 20-28) which enables the register 17 to respond to different sampling rates to generate the appropriate sine and cosine functions using the appropriate function data access by table indexing (col 4, line 53-66)**
- 4) the claimed multiplying circuit for multiplying the color difference signal by values calculated from the values of the trigonometric functions stored at the addresses specified by the address calculating circuit **is met by multiplying circuits 13 and 14 for the cosine and sine generators 18 and 19, respectively, Fig 2 (col 4, line 53-67).**

In considering claims 2 and 12, Ogawa discloses all the claimed subject matter,

- 1) the claimed value selecting circuit for selecting a predetermined value to be added in accordance with the video format actually used **is met by VAL 30 which sets an operation rate constant Fig 2, col 4, line 14-19.**
- 2) the claimed adder for adding the value to be added selected by the value selecting circuit to the addresses specified by the address calculating circuit **is met by adder 16 for adding operation constant from VAL 30 and to phase information value  $\theta$  specified by cosine and sine function generator 18 and 19 respectively (Fig 2, col line 14-19).**
- 3) the claimed flip-flop circuit for temporarily storing values output from the adder and refreshing those values in synchronism with regular clock pulses so that the address are refreshed with those values **is met by register 17 (Fig 2) which stores the output values from adder 16 in synchronization with the clock Cck (Fig 2) (col 3, line 13-16)**

In considering claim 8, Ogawa discloses all the claimed subject matter,

The claimed a luminance signal generating circuit for generating a luminance signal from the RGB signals **is met by matrix 10 which generates a luminance signal from the RGB input signals (Fig 2).**

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 4, 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ogawa et al., US 4,982,179**.

In considering claims 4 and 9, Ogawa does not specifically disclose the use of an adder circuit to obtain a carrier chrominance signal.

1) the claimed wherein the color-difference signal includes color-difference signals B-Y and R-Y **is met as shown in Fig 3 output from matrix 10**

2) the claimed wherein the values of the trigonometric functions include values of sine and cosine functions **is met by cosine and sine function generator 18 and 19 (Fig 3) (col 4, line 53-67)**

3) the claimed a first multiplying circuit for multiplying the color-difference signal B-Y by the values of the sine function **is met by sine generator 19 which inputs values to multiplier 14 (Fig 3)**

4) the claimed a second multiplying circuit for multiplying the color-difference signal R-Y by the values of the sine function **is met by cosine generator 19 which inputs values to multiplier 15 (Fig 3)**

5) the claimed adding circuit for adding an output of the first multiplying circuit to an output of the second multiplying circuit to obtain a carrier chrominance signal **is met by adder 20 which adds the outputs from multipliers 13 and 14 (Fig 3)**

**Ogawa discloses the use of adder 20 which adds the carrier chrominance signal with the luminance signal (Fig 2) to obtain a composite video signal.**

Ogawa illustrates in Prior Art drawing Fig 1, which utilizes two adders, one (9a) to obtain the carrier chrominance signal and the two (9b) to obtain the composite (chrominance + luminance) signal.

Therefore, it would be obvious to one skilled in the art to recognize that by separating the function of a single adder that adds the carrier chrominance signal and luminance signal as done in (Fig 1) would perform the same function as a separate adder (Fig 2).

In considering claim 7, Ogawa does not specifically disclose PAL, PAL-M, PAL-N format in the claimed the value to be added has a different value depending on whether an NTSC, PAL, PAL-M or PAL-N format is used.

The examiner takes "OFFICIAL NOTICE" in regards to an encoder which provides a different value depending on the format (PAL, PAL-M/N) being used. Although, Ogawa only discloses the use of an NTSC which is a standard format used in the United States and PAL is a standard format used in Europe. The use of encoders which process various standards to include PAL, NTSC, SECAM, HDTV and EDTV are well-known in the art in order to provide a system the ability to display multiple broadcast standard signals. Therefore, it would be obvious to one skilled in the art to recognize that various signal formats (NTSC and PAL or others systems) can be used as disclosed by applicant (page 1, line 10-14).

***Allowable Subject Matter***

Art Unit: 2614

9. Claims 3 and 5-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter: Prior Art does not show the following:

Claim 3: A shift circuit for dividing the addresses output from the flip-flop circuit by a shift operation.

Claim 5: An inverting circuit for inverting the polarity of the values of the cosine function, a switch for feeding the second multiplying circuit alternately with the values of the cosine function.

### ***Conclusion***

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. **Mukai, US 5,638,135; Nikoh, US 5,406,335 and Kobayashi, US 5,365,275.**

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Yenke whose telephone number is (703) 305-9871. The examiner can normally be reached Monday-Thursday from 7:00am to 5:30pm.

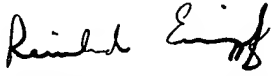


Art Unit: 2614

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Reinhard J. Eisenzopf, can be reached at (703)305-4711. The fax number for this Group is (703)308-6306 or 6296.

B.P.Y.

25 APRIL 2001

  
REINHARD J. EISENZOPF 5-6-01  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600